

**WHAT IS CLAIMED IS:**

1. A substrate layout method for reducing cross talk of adjacent signals, the substrate having a plurality of signal pads formed on a die, a ring around said die, and a plurality of signal fingers around said ring, the substrate layout method comprising:
  - forming a guard pad between two adjacent signal pads;
  - forming a guard finger between two adjacent signal fingers;
  - forming a first bonding wire to connect said guard pad to said ring;
  - forming a second bonding wire to connect said ring to said guard finger; and
  - forming a guard trace to connect said guard finger to a via at the edge of the substrate, and connecting said guard trace to a short-circuiting place through said via.
2. The substrate layout method as claimed in claim 1, wherein the substrate is a ball grid array.
3. The substrate layout method as claimed in claim 1, wherein said guard pad is selected from the group consisting of a power and ground pad.
4. The substrate layout method as claimed in claim 1, wherein said ring is selected from the group consisting of a power and ground ring.
5. The substrate layout method as claimed in claim 1, wherein said short-circuiting place is selected from the group consisting of a power and ground plane of the substrate.
6. The substrate layout method as claimed in claim 1, wherein said short-circuiting place is selected from the group consisting of a power and ground solder ball under the substrate.
7. A substrate layout structure for reducing cross talk of adjacent signals, the substrate having a plurality of signal pads formed on a die, a ring around said die, and a plurality of signal fingers around said ring, the substrate layout structure comprising:
  - a guard pad formed between two adjacent signal pads;
  - a guard finger formed between two adjacent signal fingers;
  - a first bonding wire for connecting said guard pad to said ring;
  - a second bonding wire for connecting said ring to said guard finger; and
  - a guard trace for connecting said guard finger to a via at the edge of the substrate, and connecting said guard trace to a short-circuiting place through said via.

1 8. The substrate layout method as claimed in claim 7, wherein the substrate is a ball  
2 grid array.

1 9. The substrate layout method as claimed in claim 7, wherein said guard pad is  
2 selected from the group consisting of a power and ground pad.

1 10. The substrate layout method as claimed in claim 7, wherein said ring is selected  
2 from the group consisting of a power and ground ring.

1 11. The substrate layout method as claimed in claim 7, wherein said short-circuiting  
2 place is selected from the group consisting of a power and ground plane of the substrate.

1 12. The substrate layout method as claimed in claim 7, wherein said  
2 short-circuiting place is selected from the group consisting of a power and ground solder  
3 ball under the substrate.

1 13. A substrate layout method for reducing cross talk of adjacent signals, the substrate  
2 having a plurality of signal pads formed on a die, a ring around said die, and a plurality of  
3 signal fingers around said ring, the substrate layout method comprising:

4 forming a guard finger between two adjacent signal fingers;

5 forming a bonding wire to connect said ring to said guard finger; and

6 forming a guard trace to connect said guard finger to a via at the edge of the  
7 substrate, and connecting said guard trace to a short-circuiting place through said via.

1 14. The substrate layout method as claimed in claim 13, wherein said ring is selected  
2 from the group consisting of a power and ground ring.

1 15. The substrate layout method as claimed in claim 13, wherein said short-circuiting  
2 place is a power and ground plane of the substrate.

1 16. The substrate layout method as claimed in claim 13, wherein said  
2 short-circuiting place is a power and ground solder ball under the substrate.

1 17. A substrate layout structure for reducing cross talk of adjacent signals, the substrate  
2 having a plurality of signal pads formed on a die, a ring around said die, and a plurality of  
3 signal fingers around said ring, the substrate layout structure comprising:

4 a guard finger formed between two adjacent signal fingers;

5 a bonding wire for connecting said ring to said guard finger; and

6 a guard trace for connecting said guard finger to a via at the edge of the substrate,  
7 and connecting said guard trace to a short-circuiting place through said via.

1 18. The substrate layout method as claimed in claim 17, wherein said ring is selected  
2 from the group consisting of a power and ground ring.

1 19. The substrate layout method as claimed in claim 17, wherein said short-circuiting  
2 place is selected from the group consisting of a power and ground plane of the substrate.

1 20. The substrate layout method as claimed in claim 17, wherein said  
2 short-circuiting place is selected from the group consisting of a power and ground solder  
3 ball under the substrate.

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